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Surface Photovoltage Method for Silicon-Sapphire Interface Monitoring

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***Abstract* — surface photovoltage (SPV) method was used to evaluate the silicon-sapphire interface potential barrier of silicon on sapphire (SOS) wafers obtained by CVD technique. The method provides monitoring of silicon-sapphire interface quality. Fabrication process parameters which influence on SPV signal were found. Silicon deposition temperature has a great importance on SPV signal. It was found that SPV method can be used as monitoring method of SOS fabrication process, because SPV signals are correlated with X-ray reflectometry results. Probably, SPV method is allowed to evaluate the structural and electrophysical parameters of silicon-sapphire interface. SOS device performances as function of SPV signal were determined. It was concluded that MOSFETs fabricated on SOS wafers with SPV signal above 450 mV had poor performance and MOSFETs fabricated on SOS wafers with SPV signal in range 120-320 mV had good performance.**

Keywords — surface photovoltage; SPV; silicon on sapphire; SOS; silicon-sapphire interface; interface monitoring; MOSFET.

I. Introduction

The monitoring of material parameters during fabrication process is a key for high quality product with good yield. The phenomenon of surface photovoltage (SPV) known for many years and nowadays also is used for evaluating and measuring some electrophysical parameters of semiconductor materials [1]. The SPV method is a validated contactless technique for semiconductor diffusion length characterization, which is based on the analysis of light-induced changes in the surface voltage. These changes correlate with recombination processes in silicon layer which can be interpreted as structural defects or electro-physic disorders of epitaxial layer..

Silicon on sapphire (SOS) wafers are used as base material for external impact hardness device and microwave circuit fabrication [2-4]. SOS layer contains a lot of structural defects which restrain the widespread distribution of the wafers. The structural defect concentration is not an uniform across the silicon layer. This concentration is higher near the silicon-sapphire (Si-Al_2O_3) interface and lower near the silicon surface. This factor leads to appearance of built-in potential in SOS wafers and makes possible to monitor of Si-Al_2O_3 interface quality during process fabrication. In [5] SOS wafers were measured by SPV method for investigation of structural heterogeneity in SOS layers. It was concluded that SPV method may be a measure of structural perfection of silicon-sapphire interface.

However, to our knowledge, analysis of SPV signal function of fabrication process parameters still has not done. Monitoring of SPV signal of SOS wafers during the fabrication process allows to investigate this issue.

II. Experiment

A. *Epitaxial equipment and technique*

SOS wafers are formed with vertical inductive reactor by chemical vapour deposition (CVD) technique. 4 inch single crystal sapphire R-plane wafers were used as substrates. Sapphire substrates were loaded onto carbonized graphite susceptor covered by high pure polysilicon layer. The temperature was measured via optical pyrometer at susceptor centre. The total pressure in reactor chamber was 1 atm. Dry hydrogen (the vapour water content < 5 ppb) was used as carrier gas. Silane (SiH_4) gas diluted by hydrogen (5% SiH_4 – 95% H_2) was used as precursor. Phosphine (PH_3) was used as doping (n-type) gas.

Experimental processes were carried out with different fabrication process parameters such as deposition temperature, deposition rate and doping.

B. *SPV measurements*

The schematic view of SPV measurement device is shown in Figure 1. The measuring procedure can described by several steps: illumination area of the silicon-sapphire interface to be investigated by luminous flux (LED of 430 nm wavelength) through backside of substrate, generation of electron-hole pairs by light, diffusion and redistribution of charge carriers inside silicon layer. The carrier diffusion flux approaches the boundary of the space charge region, which is always presented near the interface. The excess electrons are transferred by an electric field to the interface. Part of the electrons neutralize acceptor states and change the charge state of the Si-Al_2O_3 interface. These processes modify SPV signal of sapphire substrate which is detected by electrode and pass through an amplifier to the analytical tools where signal is treated by special software. In result, we obtain an estimate of Si-Al_2O_3 interface as SPV signal which measured in mV.

C. *Other measurement methods*

Standard quality parameters of each SOS wafers was controlled. Thickness of layer was measured by IR spectrometry (FSM 1201, Infraspek Ltd., Russia). Surface roughness was detected via UV scattering (Reflex 375, Reflex

– light Ltd., Russia). Resistivity of silicon layer was measured by four-probe method (ResMap 178, CDE Inc., USA). X-ray reflectometry (X-Ray Minilab, IRO Co Ltd, Russia) was carried out.

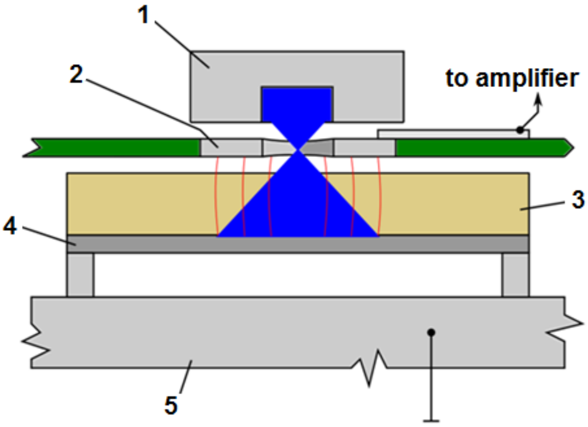

Fig. 1. Schematic view of the SPV measurement device, where 1 – light source (LED of 430 nm wavelength), 2 – transparent conductive electrode, 3 – sapphire substrate, 4 – Si layer, 5 – metallic plate.

III. Results

SOS wafers with 200 and 600 nm thickness of <100> n-type silicon layer were obtained. The wafers with 200 nm layers were used for reflectometry analysis. Thickness uniformity was ± 10% from set point. Resistivity was ± 10% from set point. Resistivity of SOS layers of experimental processes was in the range 2÷15 Ω·cm.

A. Deposition temperature

It was found there is a strict linear trend of SPV dependence on deposition temperature in series of experimental processes which carried out at different deposition temperatures. Results are shown in Figure 2.

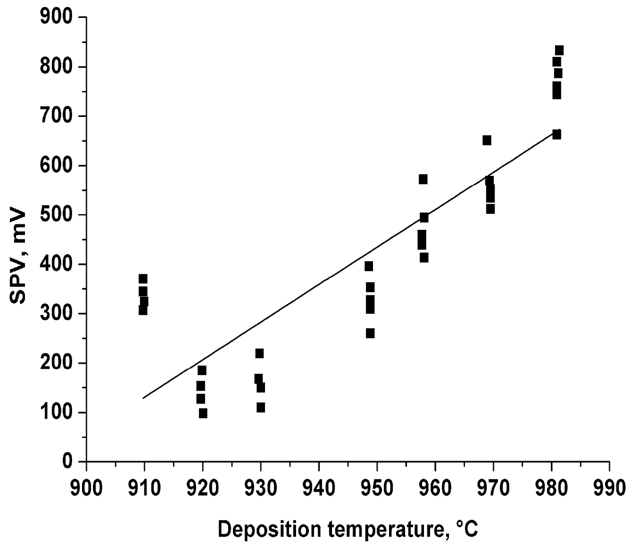

Fig. 2. Dependence of the SPV signal on SOS layer deposition temperature. Each point – SOS wafer fabricated in individual process. The data dispersion is caused by temperature measurement accuracy.

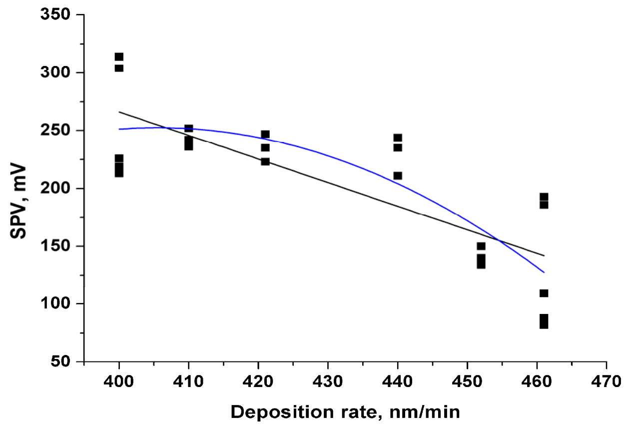

Fig. 3. Dependence of the SPV signal on SOS layer deposition rate. Each point – SOS wafer fabricated in individual process. Black line is the linear fit and blue line is the polynomial fit of second order.

The temperature range 910 – 920 °C is intermediate range between polycrystal and monocrystal silicon formation onto sapphire surface. The silicon layers had a rough surface and polycrystalline structure on samples at 910 °C. The samples having smooth surface and monocrystalline structure of layer were formed at temperatures higher than 920 °C. The SPV signal was increasing up to 980 °C. At deposition temperature about 990 °C and above the SOS layer have high defect density due to active reaction between silicon and sapphire. Probably, defect crystal structure is a reason of SPV signal increasing. High structural defect concentration near the Si-Al_2O_3 interface could change the surface charge as described in [5]. However, rising autodoping effect could be a reason of SPV signal increasing. Atomic aluminum from substrate can generate acceptor traps and modify surface charge.

B. Deposition rate

The relationships between SPV signal and deposition rate can be interpreted as linear or polynomial function as shown in Figure 3. The deposition rate was varied only by precursor gas flow rate variation in range of 400 – 460 nm/min. The deposition temperature in this processes was constant (950 °C). SPV signal of SOS wafers was decreasing while deposition rate was increasing. Probably, deposition rate increasing suppresses decomposition reaction of sapphire and aluminum autodoping by quick coverage of sapphire surface.

C. Dopant flow rate

SPV signal as function of phosphine (PH_3) flow rate is shown in Figure 4. Shown dependence has a large scatter of data but a linear trend can be traced. As known, resistivity of silicon layer depends on dopant flow rate. Phosphine flow rate was changing from 52 to 76 cm^3/min, resistivity was decreasing from 15 to 2 Ω·cm. The SPV signal was decreasing while PH_3 flow rate was increasing. The dopant flow rate increasing can change Fermi level that modify potential barrier height on the interface. On the other hand, atomic phosphor can be incorporated into the sapphire surface on the oxygen deficient regions [6] at first seconds of deposition process. Probably, this factor can decrease structural defect concentration at interface and SPV signal.

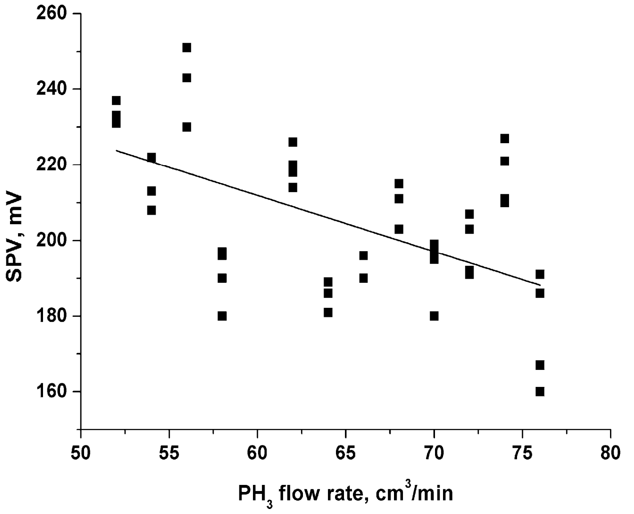

Fig. 4. SPV signal vs. PH_3 flow rate. Each point – SOS wafer fabricated in individual process. Resistivity of SOS layers in processes was decreasing from 15 to 2 Ω·cm while phosphine flow rate was increasing.

D. X-ray reflectometry

The reflectometry measurements were carried out with symmetric Bragg intensive Si (400) reflection. The reflectogram of SOS wafers with different SPV signals is shown in Figure 5. The graphic chart shows that SPV signal influences on shape of reflectogram curve.

The quantitative results of reflectometry analysis for silicon-sapphire interface are shown in Table 1. The interface was defined as transition layer between silicon and sapphire, thickness of this layer was being from 27 to 44 Å approximately.

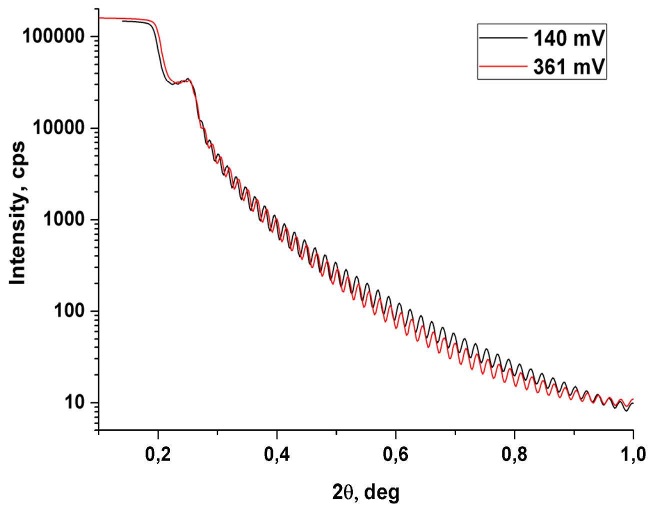

Fig. 5. Typical reflectogram of SOS wafers with different SPV signals. Scan mode – θ-2θ with angular pitch Δθ = 0,001°. Black line is the reflectogram of SOS wafer with 140 mV SPV signal. Red line is the reflectogram of SOS wafer with 361 mV SPV signal.

TABLE I. REFLECTOMETRY RESULTS FOR SILICON-SAPPHIRE INTERFACE.

SPV, mV	**Parameter of transition layer**		
	Thickness, Å	***Roughness, Å***	***Density, g/cm³***
140	28±6	13±4	2,70±0,14
259	27±8	20±4	2,75±0,14
361	34±8	24±6	2,75±0,15
643	44±6	27±6	2,75±0,15

Main parameters of transition layer obtained in this work were thickness, roughness and density. It was found that SPV signal was in correlation with thickness and roughness of transition layer.

The SPV signal increased with these two parameters. The SOS wafers with high SPV signals were fabricated with high deposition temperature (III, A). Probably, thickness and roughness increasing is caused by high deposition temperature.

E. SOS MOSFETs

Experimental SOS wafers with 600 nm Si layer were used for standard p-channel MOSFETs fabrication. The relationship between SPV signal and leakage current of test-transistors is shown in Figure 6. The leakage current of MOSFETs increased with the increasing of SPV signal. It may be due to high defect density at silicon-sapphire interface or parasitic junction presence. The transistors fabricated on SOS wafers with SPV signal above 450 mV had high leakage current value as compared with transistor fabricated on SOS wafers with SPV signal in range 120-320 mV. The leakage current had lower value and good data uniformity.

The relationship between leakage currents of MOSFETS and SPV signal allowed to use SPV method for quality control of fabricated SOS wafers.

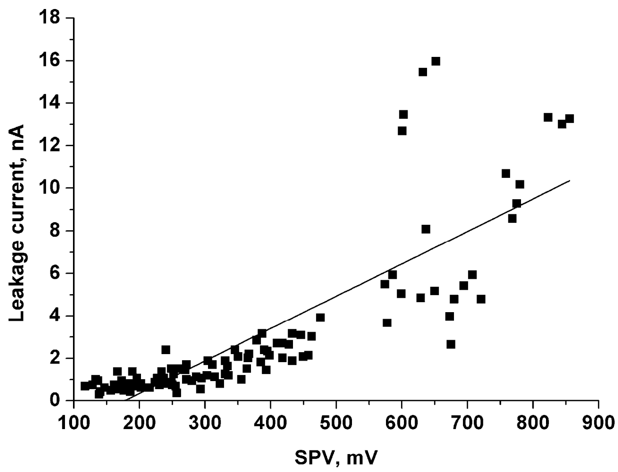

Fig. 6. SOS MOSFETs leakage current vs. SPV signal. Each point – MOSFET fabricated on SOS wafer with individual SPV signal. . Black line is the linear fit of the dependence.

IV. Conclusion

The monitoring of SOS wafers quality during fabrication process allowed to define SPV signal dependence on main fabrication process parameters. The SPV signal increases with deposition temperature. The SPV signal decreases while deposition rate and dopant (n-type) flow rate increase. These obtained dependences will enable to control the quality of SOS wafer in real-time process. It was concluded that SPV signals are in good correlation with layer resistivity (identically dopant flow rate) and reflectometry results. Reflectometry analysis allowed to estimate the transition layer between epitaxial silicon layer and sapphire substrate. SPV signal was increased with thickness and roughness of the transition layer. It was found that SPV signal is depending on structural and electrical parameters of SOS layer.

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