Hydride-Chloride Epitaxy of High-Resistivity Si-Layers on High-Doped Wafers

Evgeniy M. Sokolov, Vladimir N. Statsenko
Epiel JSC
Moscow, Zelenograd, Russia
vstatsenko@epiel.ru

Dmitry V. Tarasov, Sergey D. Fedotov
National Research University of Electronic Technology MIET
Moscow, Zelenograd, Russia
fedotov.s.d@yandex.ru

***Abstract*— High-resistivity silicon layers were deposited on different high-doped wafers with arsenic, antimony and boron doping. The Si-layers were formed at 950-1050 °C with various vapor-gas mixture composition: SiH_4, SiH_4+$SiCl_4$, SiH_4+$SiHCl_3$, $SiHCl_3$. Resistivity thickness profile was measured by spreading resistance probe (SRP) method. Unusual resistivity profile incline was detected for isotype junction. It was found that the phenomenon of doping segregation appears when Si-layers deposit on arsenic high-doped wafers. To our knowledge, arsenic segregation in relation to autodoping phenomenon was studied for the first time. It was discovered that the increase of growth rate and HCl etching procedure change the incline of SRP-profile. Pre-epitaxy wafer annealing allowed to decrease the concentration of arsenic on wafer surface.**

Keywords— silicon epitaxy; high-resistivity layer; high-doped wafer; arsenic segregation; resistivity profile; CVD; SRP

I. INTRODUCTION

Epitaxial growth carried out by the technique of chemical vapor deposition (CVD), is one of the most important processes in technology of silicon semiconductor devices, as it allows to obtain as a slightly- and high-doped layers on the surface of a semiconductor wafers. CVD epitaxy allows to obtain a sharp concentration profiles of a dopant, which is often required for silicon semiconductor devices.

This work was carried out to control the content of segregated arsenic on the surface and the suppression of As autodoping during the growth of epitaxial silicon layers by hydride-chloride technology.

It is known that n-type dopants (P, As) tend to stand out (segregate) to the growing surface. The bulk concentration of the incorporated atoms of arsenic is lower than those on the surface, by several orders of magnitude [1,2]. All this leads to the fact that the surface segregation reduces the incorporation of arsenic atoms in the epitaxial layer and segregated As atoms passivate the surface of the growth, thereby reducing the growth rate of the layer. It also slows down the surface diffusion. As a result, for example, in epitaxial layers with arsenic concentrations higher than 10^{18} cm^{-3} often have to be rougher surface and degradation of electro-physical properties [3].

Many studies have been conducted on the control of arsenic content as well as suppression of surface segregation of As in silicon during CVD epitaxy. So, in work [4] was investigated the selective growth of epitaxial layers, doped with arsenic, at atmospheric pressure and low temperature. One of the main conclusions of this research: to suppress the segregation of arsenic it is necessary to increase the rate of growth of the layer.

In [5] the authors carried out research to study the abruptness of the concentration profiles of arsenic and phosphorus in low-temperature silicon epitaxy. To establish dependency, the authors conducted a deposition, changing the rate and time of deposition, and also carried out stepwise (with a short stop) growth of silicon layers. In the result, it was found that the deposition rate does not affect the transition widths of arsenic. But more abrupt transition can be obtained by using time-varying silicon source-gas flows.

To balance incorporated arsenic atoms into the growing layer and segregated on the surface by the authors [6] was studied the process of epi silicon deposition in the temperature range from 650 °C to 1150 °C. The authors also note that the segregation ratio is greatly increased if the atmosphere of the epitaxial growth are present the chlorides. In addition, it is points out that to reduce the surface arsenic concentration, a combination of high-temperature annealing with increasing hydrogen consumption during annealing can be used.

In [7] was developed the technology of obtaining epitaxial layers with a variable profile of arsenic for varactors. According to this work, in the absence of intentional doping during growth, the arsenic doping profile in the epitaxial layer depends on only the number of segregated arsenic on the surface, i.e. the density of surface filling by arsenic. The dependence of the incorporation rate of arsenic into the growing layer from the growth rate of the layer was not detected, however, it is not excluded that in the experiments with a different set of process parameters such dependence may appear.

II. EXPERIMENT

There have been three series of Si epitaxial growth on substrates KEM-0,003 (111) with arsenic dopant, KES 0,01 (100) with antimony dopant, KDB-10 (111) with boron dopant. All the layers were deposited in the vertical epitaxial reactor PE2061 (LPE, Italy) for the covered lines of doping.

After the deposition process the structures were subjected to a visual inspection of the surface quality and thickness of the Si films was measured by fourier-transform infrared

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spectroscopy (FTIR). The resistivity profiles were measured by the spreading resistance probe (SRP) method.

In the first series (S1) of epitaxial growth, monosilane (SiH_4) or a mixture of monosilane and trichlorosilane (SiH_4+$SiCl_4$) was used as the silicon source-gas. Deposition process was carried out only on substrates KEM-0.003 at the temperature from 950 to 1010 °C. The natural oxide of Si was removed by the annealing process for 5 minutes at 1100 °C.

In the second series (S2), a mixture of monosilane and trichlorosilane (SiH_4+$SiHCl_3$) was used as the silicon source-gas. Deposition temperature ranged from 950 to 1030 °C. The removing silicon oxide conditions were the same as in the series 1. Here, during the growth process, substrates KEM-0.003, KES-0.01 (100), KDB-10 were used. To prevent the possible effect of As substrates KEM-0.003 and KES-0.01 were placed on opposite sides of the substrate holder.

For the third series (S3), trichlorosilane ($SiHCl_3$) was used as the silicon source-gas. The epitaxial growth was conducted on the same substrates and with the same arrangement of the plates on the substrate holder as in the second series. Deposition temperature varied from 1010 to 1050 °C. The annealing process was performed for 20 minutes at the deposition temperature.

III. Results and Discussion

The characteristic resistivity profiles of the epitaxial layer over the thickness in the first series (hydride-chloride technology) are shown in Fig. 1 with indication of the growth temperature (T_G) and growth rate (V_G). The structure in Fig. 1 had good surface quality (even at 980 °C).

From the above Fig. 1 shows that the obtained distribution profiles are about the same character – the resistivity growth corresponding to the transition zone base-layer, to a value of approximately 0.1 Ω×cm, then no charactering for isotype transitions change in the slope of the profile.

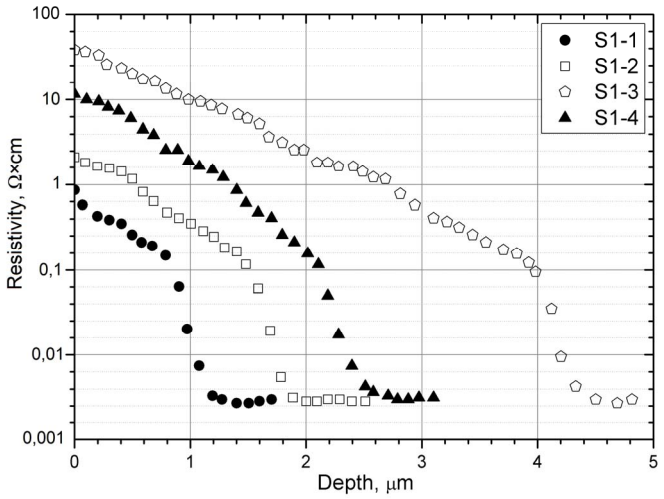

Fig. 1 Resistivity profiles of the S1 for processes: S1-1 – T_G = 980 °C, V_G = 0,08 μm/min, only SiH_4 was used as precursor; S1-2 – T_G = 1010 °C, V_G = 0,16 μm/min; S1-3 – T_G = 1030 °C, V_G = 0,19 μm/min; S1-4 – T_G = 1050 °C, V_G = 0,28 μm/min.

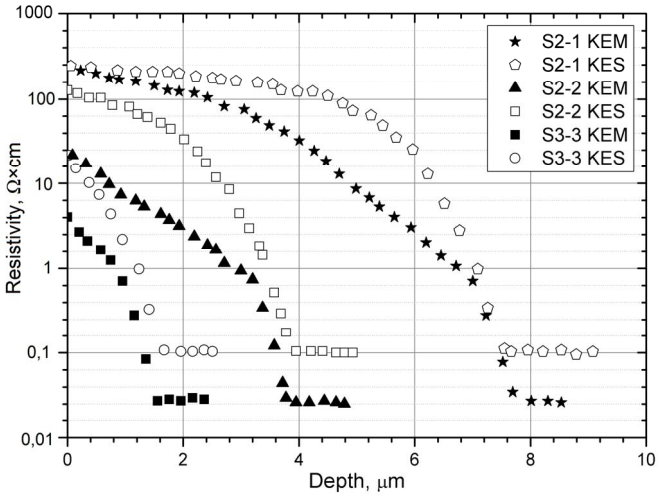

Fig. 2 Resistivity profiles of the S2 for processes: S2-1 – T_G = 950 °C, SiH_4 SiH_4+$SiHCl_3$ mixture was used as precursor, 50% vol. of $SiHCl_3$; S2-2 – T_G = 950 °C, SiH_4 SiH_4+$SiHCl_3$ mixture was used as precursor, 25% vol. of $SiHCl_3$;. S2-1 – T_G = 980 °C, only SiH_4 was used as precursor.

In the case of processes S1-1, S1-2 and S1-4, which were obtained at different temperatures, the resistivity distribution is the same, if you bring them to the same thickness (regardless of the deposition temperature). The profile of the process S1-3 is slightly different (maximum the V_G for this series), but it is unclear why the slope of profiles decreases. It is uncertain what happens to the arsenic profiles and how to manage it. Perhaps a lower temperature will allow changing something in the dopants distribution in the growing layer.

The second series of experiments was carried out using a mixture of SiH_4+$SiHCl_3$ and only $SiHCl_3$. The processes were performed at 950-980 °C (chloride-hydride technology), 980-1030 °C (only trichlorosilane). The deposition temperature and conditions of pre-epitaxial annealing remained unchanged. In addition to KEM-0.003, KES-0.01 and KDB-10 plates were loaded in each process. The curves of the resistivity are shown in Fig. 2. As can be seen from the above data, there are no fundamental changes in the resistivity profiles, despite the decreasing deposition temperature and the changing in the content of trichlorosilane in the gas mixture. It should be noted that when using hydride-chloride technology at temperatures ranging 950-980 °C, all epi layers grown on orientation substrates (111) had a matte surface; all structures on the wafers of the KES-0,01 (100) had normal quality of the surface even at 950 °C (in general, all in accordance with the growth theory of single-crystal films).

The results of fabricating structures with the use of trichlorosilane are better than in the case of chloride-hydride technology as shown in Fig. 3. But the same form of arsenic profile is preserved as in all previous structures. Somewhat the structure of S2-5 falls out of this sequence (the growth temperature is 1010 ° C, the surface is free of matte, the resistivity at the surface of the samples is 320-350 Ω×cm). The reasons for such deviations are not yet clear.

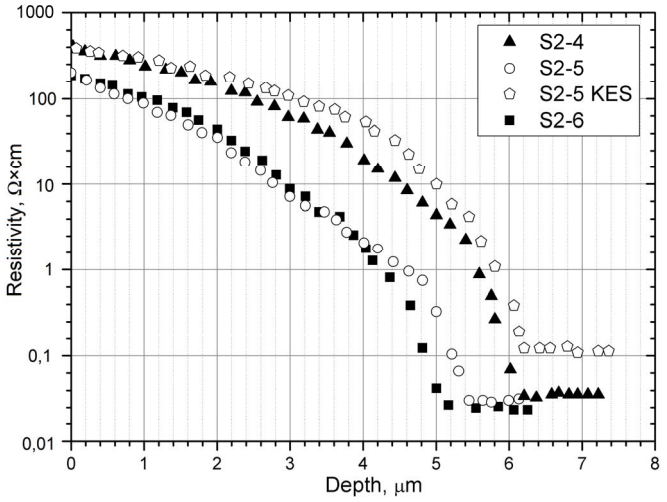

Fig. 3 Resistivity profiles of the S2 for processes where only $SiHCl_3$ was used as precursor: S2-4 – T_G = 980 °C, S2-5 – T_G = 1010 °C, S2-6 – T_G = 1030 °C.

Given the results in the study of the first microns of the growing layer it can be seen that during the epi growth on arsenic high-doped wafers, the phenomenon of impurity segregation takes place. This phenomenon has been studied in sufficient detail in the literature, but, basically, in attempt of a doping of silicon layers an arsenic during the growth. However, it is poorly studied as an autodoping source of epitaxial layers. The main recommendations for suppression of this autodoping type are reducing the deposition temperature and growth pressure. Apparently, these recommendations are based on the assumption that the main source of autodoping is arsenic, which evaporates both from the surface of the plate and from the snap surface, where it can get during pre-epitaxial annealing.

The third series of experiments was carried out using only the trichlorosilane as the silicon source, since there was the assumption that the monosilane did not have a sufficient degree of purity to obtain high-resistance layers.

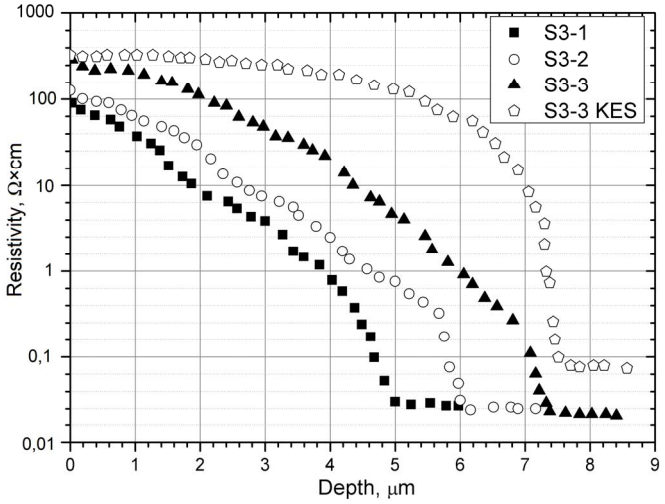

Fig. 4 Resistivity profiles of the S3 for processes at T_G = 1010 °C: S3-1 – Q_{SiHCl3} = 2 l/min, S3-2 – Q_{SiHCl3} = 4 l/min, S3-3 – Q_{SiHCl3} = 6 l/min.

Before conducting processes of this series setting was trained in accordance with the existing procedure of equipment preparation for obtaining high-resistance epitaxial layers (using a test line feeding $SiHCl_3$).

Deposition temperature ranged from 1010 to 1050 °C, while pre-epitaxial annealing is carried out at growth temperature to prevent the spread of arsenic on the surface of the substrate holder. There was also a series of processes with a change in the rate of growth of the epitaxial layer at a constant temperature increase.

In Fig. 4 shows the resistivity profiles of the layers obtained at 1010 °C and different $SiHCl_3$ flow rate (Q_{SiHCl3}). As in the previous two series radical changes of the distribution of arsenic on the thickness of the epitaxial layer does not occur.

It should be noted that with the increasing of the flow rate of $SiHCl_3$ at 1010 °C increases the haze of the obtained layers. At a temperature of 1010 °C there is a strong haze in the $SiHCl_3$ flow of 6 liters per minute (increase of specific resistance on sample S3-3 is associated with an increase in defective layer. This is the limit of the rate of growth of epitaxial layers at this temperature (0.3 μm/min for 1010 °C).

In addition, in this series conducted separate experimental processes to test the possible dependence of the rate of segregation as a possible cause of the distortion profile impurities, from various technological factors: the process with pre-annealing of the wafers for 1 hour at the deposition temperature (S3-4); the process in which the epitaxial layer was carried out in three stages, between which were carried out the annealing of the structures (S3-5) or polishing etching (S3-6) of the surface of wafers at a temperature 1120 °C at a depth of about 0.1 μm (Fig. 5).

Considering the data of Fig. 5 it is worth noting that the increase in annealing time to 1 hour at the temperature of deposition has not led to any positive result, as well as three-stage deposition of the epitaxial layer with the interim annealing and purging the reactor.

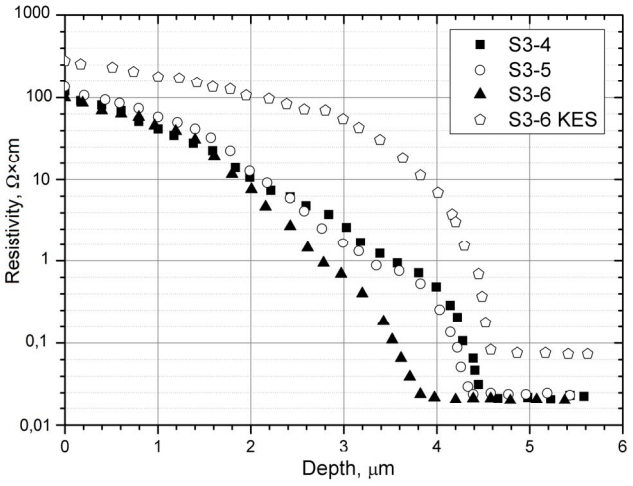

Fig. 5 Resistivity profiles of the S3 for experimental processes (T_G = 1030 °C and Q_{SiHCl3} = 4 l/min for all): S3-4 – pre-annealing of the wafers for 1 hour at T_G, S3-5 – three stages process with annealing for 5 min between stages, S3-6 – three stages process with HCl etching at 1120 °C between stages.

But the use of three-stage growth with intermediate HCl etching of the epitaxial layer has led to a more intensive increase of the resistivity, i.e. it is possible that the etching is the removal of part of the segregated arsenic from the surface layers. Probably it is necessary to check the following series of experiments.

IV. Conclusions

As the temperature of preliminary annealing for possible reduction of the distribution of arsenic in reactor and reduce autodoping (series of experiments the second and third) is that the most possible the resistivity of the layer is smaller.

The use of an intermediate of HCl etching has a useful effect on the distribution profile of the impurity (it is still necessary to repeat).

Increase the speed of layer growth has a weak effect, but still the influence of et on the distribution profile. It makes sense to try increase the rate of growth over a wide range (up to 1 μm/min).

The next series of experiments it makes sense to hold using more intensive annealing (higher temperature and duration) to reduce surface arsenic concentrations.

Acknowledgment

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