Temperature Dependence of Silicon on Sapphire Quality

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***Abstract*—Thin (300 and 600 nm) epitaxial silicon layers were deposited on R-plane sapphire wafers by CVD technique using SiH_4 and $SiCl_4$ mixture gas diluted by hydrogen. Quality parameters of epitaxial silicon on sapphire (SOS) wafers were studied by means of XRD, AFM, UV scattering and surface PV methods. Resistivity profiles of layers were measured. Quality of SOS in dependence on initial growth (up to 80-100 nm thickness of layer) temperature and growth (up to necessary thickness) temperature was observed. Optimal temperature ranges of layer growth were experimentally estimated. Using of low growth temperature (about 945-960 °C) of initial layer growth and high growth temperature (above 960 °C) of residual layer allowed to enhance quality of SOS wafer and get uniform resistivity profile of layer. Practical application of this technique allowed to produce SOS wafers of high quality in wide optimal temperature range, increase thermal stability of SOS and process efficiency.**

Keywords—epitaxial wafers; silicon on sapphire; silicon on insulator; SOS; SOI; growth temperature; epitaxial growth; initial layers growth; epitaxy; heteroepitaxy; CVD

I. INTRODUCTION

Thin silicon on sapphire (SOS) layers are used as microchip fabrication in wide function range but mostly for external impact hardness device and microwave circuit applications [1], [2]. The electronic components produced from SOS have many advantages such as high transmission speed and integration density, extended memory capacity, radiation hardness and thermal stability in comparison to analogues from bulk silicon [3]. However, SOS contains a lot of structural defects which result in degradation of electronic properties of the silicon layer. This reason constrains the widespread distribution of the SOS.

As is known polycrystalline or imperfect silicon epitaxial layer are formed when adatom migrations were forced during growth. This happens if the deposition rate is too high or the growth temperature is too low [4]. Therefore low deposition rate and high growth temperature can provide fabrication single-crystal epitaxial silicon layer with high structural and electrophysical quality. However, in case of SOS deposition process the low deposition rate and high growth temperature can cause higher aluminum autodoping from sapphire substrate to silicon layer. Therewith sapphire decomposition products pollute the epitaxial layer and generate defects on silicon-sapphire ($Si–Al_2O_3$) interface.

In SOS fabrication process by chemical vapor decomposition (CVD) there is a narrow growth temperature range which provide optimal quality of SOS wafers. Carrying out the process out of this range leads to degradation of SOS quality. The detailed investigation of quality temperature dependence can provide the estimation of optimal growth temperature and developing of new approach of SOS fabrication process which result in high production quality and thermal stability.

II. EXPERIMENT

Single crystalline epitaxial silicon layers were deposited on 4`` R-plane sapphire (α-Al_2O_3) substrates. Front surface of substrate was epi-ready polished with R_a < 0,5 nm. Set point silicon layer resistivity was in the range 1÷15 Ω·cm. Resistivity profile was measured in lightly doped SOS wafers.

A. Epitaxial equipment and technique

Heteroepitaxial layers are formed with vertical inductive reactor by chemical vapour deposition (CVD) technique. Sapphire substrate were loaded onto carbonized graphite substrate susceptor covered by high pure polysilicon layer. The temperature was measured via optical pyrometer in susceptor centre. The total pressure in reactor chamber was 1 atm. Dry hydrogen (the vapour water content < 5 ppb) was used as carrier gas. Silane (SiH_4) and silicon tetrachloride ($SiCl_4$) mixture gas diluted by hydrogen (5% SiH_4 – 1% $SiCl_4$ – 94% H_2) are used as precursors. Phosphine (PH_3) was used as doping (n-type) gas.

B. Fabrication process

The fabrication process consisted of several steps: 1) reactor chamber is purged by N_2 and H_2 2) heat up (to 1100-1200 °C) and anneal sapphire substrates in hydrogen; 3) cool down to initial growth temperature and deposition of initial silicon layer up to thickness 50-100 nm; 4) interrupting the deposition and heat treatment; 5) heat up or cool down to SOS growth temperature and deposition silicon layer to necessary thickness; 6) cool down and purge reactor chamber. Experimental processes series on search optimal growth temperatures of steps 3 and 5 were carried out. The experimental range of initial growth temperature (step 2) was 930-975 °C, of growth temperature (step 4) was 960-1005 °C. More than one hundred experimental processes were carried out for the investigation of this new approach.

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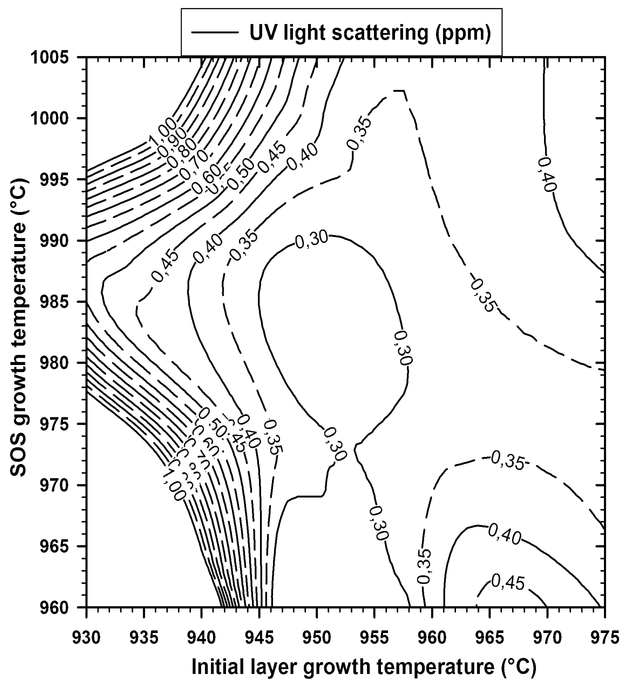

Fig. 1 Contour diagram of the UV light scattering as a function of the initial layer growth temperature and SOS growth temperature. Above 1 ppm – defective SOS layer, about 0,5 ppm – normal quality, and less 0,35 ppm – extremely high quality of SOS front surface.

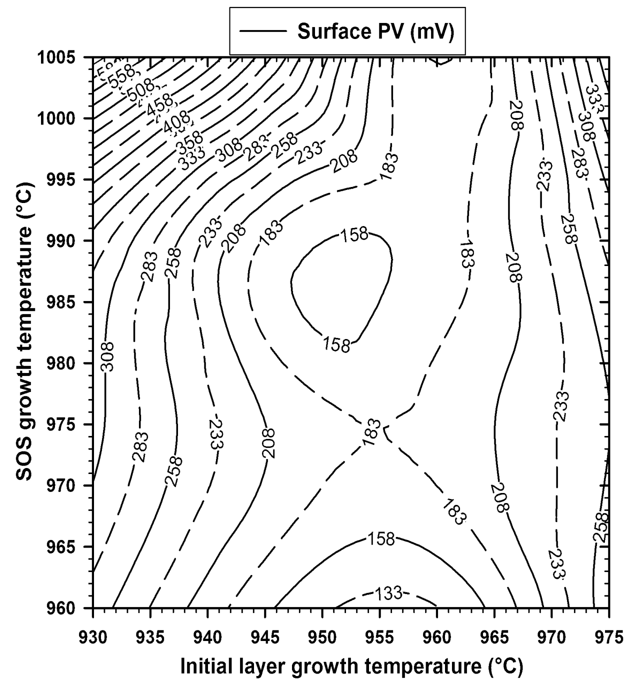

Fig. 2 Contour diagram of the surface PV as a function of the initial layer growth temperature and SOS growth temperature. Above 400 mV – defective Si-Al_2O_3 interface, poor quality, about 300 mV – normal quality, and less 200 mV – low defect density of Si-Al_2O_3 interface, high quality of SOS.

C. Measurement methods

Structural and electrophysical performances of SOS wafers were estimated by several methods. First, structural quality of Si–SiO_2 (native) and Si–Al_2O_3 interfaces were estimated via express methods. UV scattering method comprising of front surface scanning was used for Si–SiO_2 quality estimation. Surface photovoltage (PV) method was used for estimation Si–Al_2O_3 interface. Thereafter the quality of SOS layers was confirmed by AFM (Solver Pro, NT-MDT JSC, Russia) and XRD (X-Ray Minilab, IRO Co Ltd, Russia) methods. The spreading resistance probe method (SRMS SSM 130) was used for resistivity profile in lightly doped SOS wafers.

III. Results

Silicon on sapphire wafers with 300 and 600 nm layers were obtained. Thickness uniformity was ± 8% from set point. Resistivity was ± 10% from set point. Resistivity of lightly doped SOS wafer was 250÷300 Ω·cm.

A. SOS quality v.s. growth temperature

The initial growth and SOS growth temperature dependence on Si–SiO_2 interface quality is shown in fig. 1. The initial growth temperature in range approximately 945-960 °C and growth temperature above 960 °C result in small value of UV scattering that confirms high quality of SOS wafers.

The initial growth and SOS growth temperature dependence on Si–Al_2O_3 interface quality is shown in fig. 2. It was found that high and stable quality of SOS can be obtain in range ~ 945-965 °C of initial temperature growth and SOS growth temperature above 960 °C. The dependence shows that the initial growth temperature has a great influence on Si–Al_2O_3 interface quality.

As we know, standard process of SOS fabrication does not allow growth temperature about or higher 1000 °C due to Si and Al_2O_3 reacting and extremely high autodoping. However, fig. 1 and 2 show that initial growth temperature about 955 °C allows to higher SOS wafer quality in wide growth temperature range. The initial growth temperature in range approximately 945-960 °C and growth temperature above 960 °C result in small value of UV scattering that confirms high quality of SOS wafers. According to data shown in fig. 1 and 2 we can conclude that SOS growth temperature can be even higher than 1000 °C.

B. Surface roughness

The AFM results are shown in fig 3. The AFM image shown that SOS wafers obtained at optimal conditions have smooth surface with RMS roughness less 0,9 nm. High quality of Si–SiO_2 interface was confirmed by AFM.

C. Structural quality

The rocking curve measurements were carried out for symmetric Brag intensive Si (400) reflection. The rocking curves for SOS wafers with thickness 300 and 600 nm are shown in fig 4. FWHM of 600 nm SOS layers was approximately 0,25 °, of 300 nm – 0,35 °. All wafers were made with optimal conditions.

Structural perfection of SOS layers was confirmed by XRD measurements. The wafers have high structural quality which confirmed by [5] wherein SOS wafers were fabricated by standard CVD process using diluted SiH_4 as precursor.

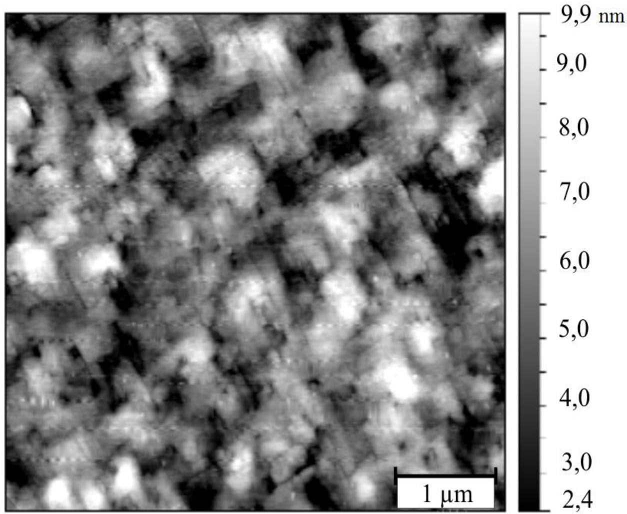

Fig. 3 Typically AFM image of SOS wafer surface formed at optimal growth temperatures. The right scale is a surface microrelief height.

D. *Resistivity profile*

Fig. 5 shows typically resistivity profile of lightly n-type doped SOS wafers. Low initial growth temperature (about 945-960 °C) reduces aluminium (p-type doping) diffusion. The initial silicon layer has low aluminium concentration and blocks autodoping during subsequent silicon deposition even with high SOS growth temperature (about 1000 °C). It has been observed that further usage of high growth temperature (about 980-990 °C) provides high quality of layers without autodoping increase. Resistivity profile of lightly n-type doped SOS wafer on fig. 5 very smooth until a depth approximately 3000-3500 Å. Resistivity increases at a depth about 2000 Å in standard SOS process. It also suggests that the use of the new method increases the thermal stability of SOS fabrication process. This will lead to increase the quality uniformity (in one process) and good yield of SOS wafers.

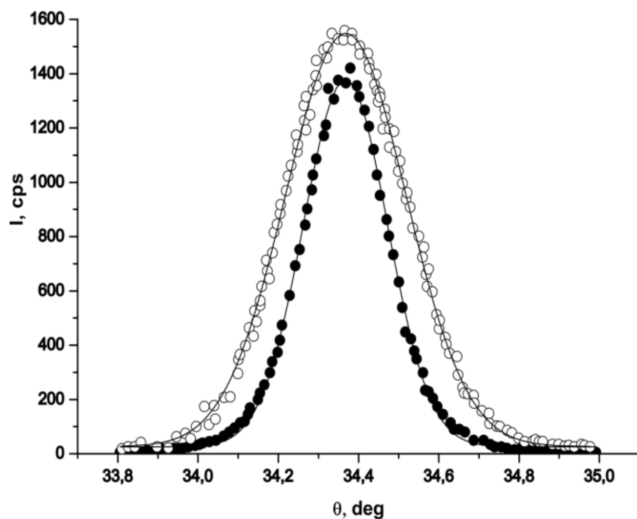

Fig. 4 Typically rocking curves of SOS layers formed at optimal growth temperatures. The curves indicated on the graph: ○ – 300 nm thickness layer; ● – 600 nm thickness layer.

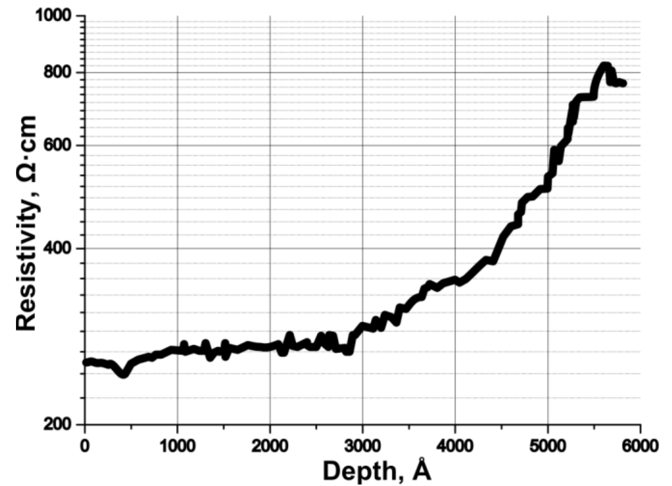

Fig. 5 Typically resistivity profile of lightly doped SOS wafers. The graph show reduce autodoping from substrate using low initial growth temperature and higher growth temperature of fabrication process.

IV. CONCLUSIONS

New approach to SOS fabrication process (II, B) was tested. The fabrication processes of SOS wafers with layer thickness 300 and 600 nm were carried out, SOS wafers quality was investigated, process efficiency was approved. Structural quality dependence as function of growth temperature was experimentally obtained and analyzed. It was found that initial growth temperature in range ~ 945 – 960 °C and SOS growth (to desirable thickness) temperature above 960 °C provided high Si–SiO_2 interface quality. The initial growth temperature about 955 °C provided high Si–Al_2O_3 interface quality on wide growth temperature range (even above 1000 °C). SOS growth temperature range 980-990 °C provides high structural perfection of silicon layer. AFM and XRD study of SOS allowed the support of the experimental results. RMS roughness of SOS surface was less 0,9 nm. FWHM of 600 nm SOS layers was 0,25 °, of 300 nm – 0,35 °. The studies SOS wafers obtained at optimal conditions by new approach. Uniform resistivity profile of lightly doped 600 nm SOS wafers was obtained. The initial growth temperature range (935-955 °C) blocks autodoping from sapphire substrate during SOS layer deposition and obtains very smooth resistivity profile until a depth approximately 3000-3500 Å.

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